IN THE CLAIMS

Please replace the pending claims with the following set, in which claim 5 has been amended and claims 10-17 are new.

1-4 (Withdrawn)

5. (Amended Four Times) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

an impurity implantation region of impurities of a second conductivity type formed in a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

the impurity implantation region of the first sector comprising a depletion channel of the second conductivity type occupying a surface region of the semiconductor substrate [second conductivity type as a depletion channel];

a second sector of the channel region exclusive of the first sector comprising [a] an enhancement channel of the first conductivity type with uniform doping concentration [of the first conductivity type] and occupying a surface region of the [first conductivity type as an enhancement channel] semiconductor substrate;

a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

6. (Original) The transistor of claim 5, wherein the first sector has a narrower line width than a line width of the gate.

7. (Previously Amended) The transistor of claim 5, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

8. (Previously cancelled)

9. (Original) The transistor of claim 5, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.

10. (New) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

an impurity implantation region formed on the semiconductor substrate, having impurities of a second conductivity type, and with a lateral extent coextensive with the first sector, the impurity implantation region further comprising a first surface region that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate within the first sector;

a second sector of the channel region exclusive of the first sector, the second sector comprising a second surface region that functions as an enhancement channel, that occupies an entire surface of the semiconductor substrate in the second sector, and that has uniform doping concentration of the first conductivity type;

a gate insulating layer on the substrate over at least a portion of the first surface region and the second surface region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

a second sector of the channel region exclusive of the first sector comprising an enhancement channel of the first conductivity type with uniform doping concentration and occupying a surface region of the semiconductor substrate;

a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

11. (New) The transistor of claim 10, wherein the first sector has a narrower line width than a line width of the gate.

12. (New) The transistor of claim 10, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

13. (New) The transistor of claim 10, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.

14. (New) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

an impurity implantation region formed on the semiconductor substrate, having impurities of a second conductivity type, and with a lateral extent coextensive with the first sector, the impurity implantation region further comprising a first surface region that functions as a depletion channel and that occupies the entire top surface of the semiconductor

substrate within the first sector, the first surface region having a top surface and a bottom surface, wherein the top surface is larger than the bottom surface;

a second sector of the channel region exclusive of the first sector, the second sector comprising a second surface region that functions as an enhancement channel, that occupies an entire surface of the semiconductor substrate in the second sector, and that has uniform doping concentration of the first conductivity type;

a gate insulating layer on the substrate over at least a portion of the first surface region and the second surface region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

15. (New) The transistor of claim 10, wherein the first sector has a narrower line width than a line width of the gate.

16. (New) The transistor of claim 10, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

17. (New) The transistor of claim 10, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.